

CMOS BEAMFORMING TECHNIQUES

PROJECT OVERVIEW

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Computer Architecture for Embedded Systems (CAES)

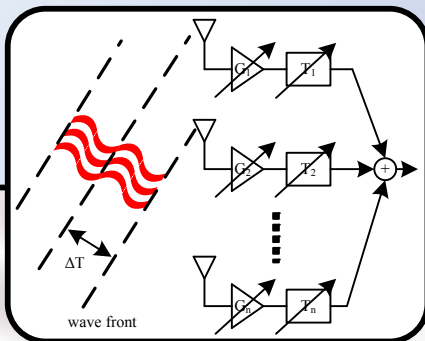
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Integrated Circuit Design (ICD)

BEAMFORMING PRINCIPLE

- Wavefront arrives at antennas at different times
- Compensate for time delay
 - Can be done at RF, IF or digital

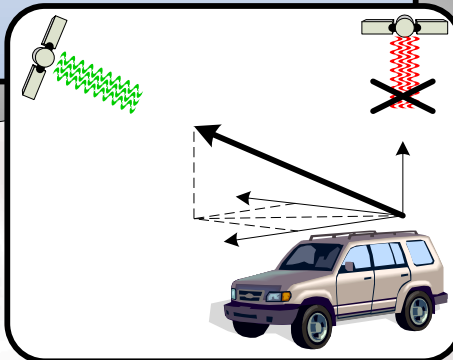


PROJECT GOALS

- Explore fundamental options for beamforming
- Beamforming architecture suitable for CMOS
 - Analog: phase shifters, time delay, RF processing
 - Digital: reconfigurable processing
 - Combine analog and digital advantages

RESEARCH APPLICATION

- DVB satellite receiver for mobile situations
 - Beamforming based on car/satellite position
 - Receive signal from multiple satellites
 - Reject interference from other transmitters



CHALLENGES

- CMOS phase/time shifter
- Feasibility of the ADC
- RF/IF conversion
- Flexible digital processing
- On-chip/off-chip communication

Component type	RF hybrid	CMOS
Microwave structures	++	--
Inductor	+	□
Capacitor	+	+
RF-Transistor	□	+
Digital logic gates	□	++

APPROACH

- Analysis of system requirements
- A/D partitioning
- Architecture exploration
- Implementation *Design 1*
- Evaluation *Design 1*
- Implementation *Design 2*
- Chip fabrication and evaluation

PROPOSED SYSTEM ARCHITECTURE

- Phased array consisting of 10's to 1000's of antennas
- Architectural possibilities
 - Topology: tile based, hierarchical
 - Processing: analog beamforming of multiple antennas followed by single ADC, further processing digitally with reconfigurable processors (RP)

